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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/628,500	07/28/2003	Makoto Miyazawa	NEKU 20.544	5066

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EXAMINER	
NGUYEN, KHIEM D	
ART UNIT	**PAPER NUMBER**
2823	

DATE MAILED: 06/28/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/628,500	MIYAZAWA ET AL.	
	Examiner	Art Unit	
	Khiem D. Nguyen	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 July 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3 and 7-18* is/are rejected.

7)☒ Claim(s) *4-6* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *28 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *07/28/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Information Disclosure Statement

The Information Disclosure Statement filed on July 28th, 2003 has been considered.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-3 and 7-18 are rejected under 35 U.S.C. 102(e) as being anticipated by Matsui (U.S. Patent 6,507,232).

The applied reference has a common assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not the invention "by another," or by an appropriate showing under 37 CFR 1.131.

In re claim 1, **Matsui** discloses a semiconductor integrated circuit device comprising: a terminal **100**; and a first capacitance adjusting section **103** which is connected to a wiring between the terminal and a protection resistor **101** in front stage of an internal circuit **111** (col. 7, line 39 to col. 8, line 65 and FIG. 3),

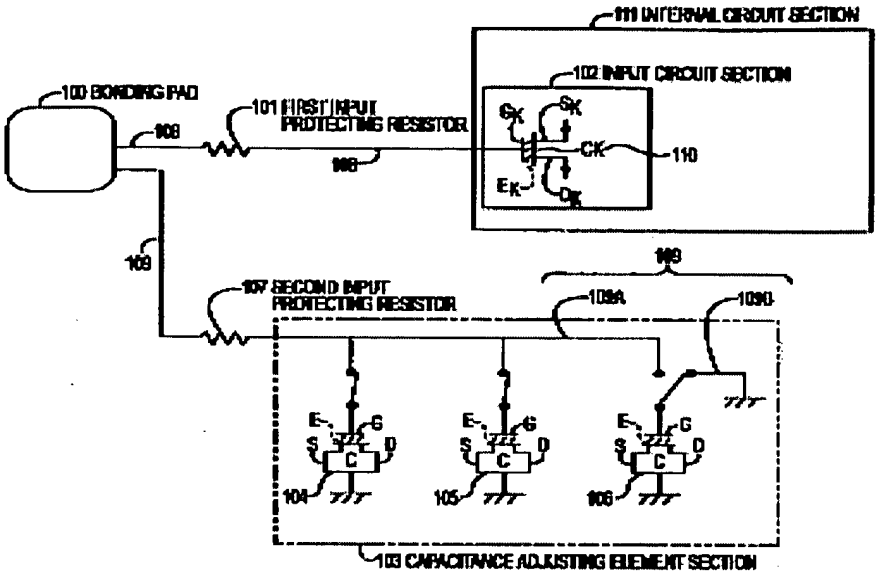
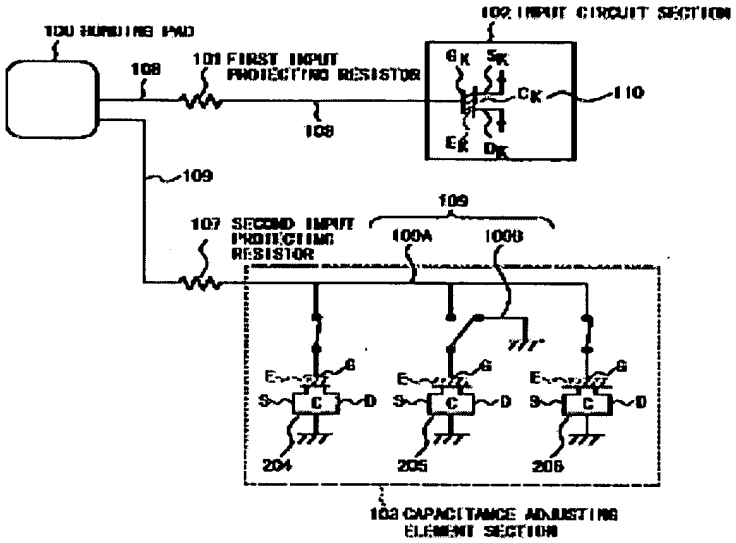


FIG. 3

wherein the first capacitance adjusting section adjusts terminal capacitance of the terminal, based on capacitance of the first capacitance adjusting section (col. 7, line 39 to col. 8, line 65).

In re claim 2, **Matsui** discloses that the semiconductor integrated circuit device according to Claim 1, further comprising: a protection circuit which is connected to the wiring between the adjusting terminal and the first capacitance section and protects the internal circuit (FIG. 4).

Fig. 4



In re claim 3, **Matsui** discloses that the first capacitance adjusting section comprises a first adjusting capacitor which adjusts the terminal capacitance (col. 7, line 39 to col. 8, line 65 and FIG. 3),

the first adjusting capacitor comprises: a first semiconductive portion which is composed of a first well region formed in a substrate with the internal circuit and having a conductive type opposite to that of the substrate, and a second semiconductive portion which is opposite to the first semiconductive portion and is composed of a first diffusion layer region formed in the first well region and having the same conductive type as that of the substrate (col. 7, line 62 to col. 8, line 39 and FIG. 4).

In re claim 7, **Matsui** discloses that the first capacitance adjusting section comprises a first adjusting capacitor which adjusts the terminal capacitance, the first adjusting capacitor comprises: a first semiconductive portion which is composed of a first well region formed in a substrate with the internal circuit and having a conductive type

opposite to that of the substrate, and a second semiconductive portion which is opposite to the first semiconductive portion and is composed of a first diffusion layer region formed in the first well region and having the same conductive type as that of the substrate (col. 7, line 62 to col. 8, line 39 and FIG. 4).

In re claim 8, **Matsui** discloses that the semiconductor integrated circuit device according to Claim 7, further comprising: a well potential control section wherein the first capacitance adjusting section further comprises a second adjusting capacitor which adjusts the terminal capacitance based on controlling a well region potential by the well potential control section, the second adjusting capacitor comprises: a third semiconductive portion which is composed of a second well region formed in the substrate and having a conductive type opposite to that of the substrate, a fourth semiconductive portion which is opposite to the third semiconductive portion and is composed of a second diffusion layer region formed in the second well region and having the same conductive type as that of the substrate, and the well potential control section controls the well region potential of the second well region (col. 7, line 62 to col. 8, line 39 and FIG. 4).

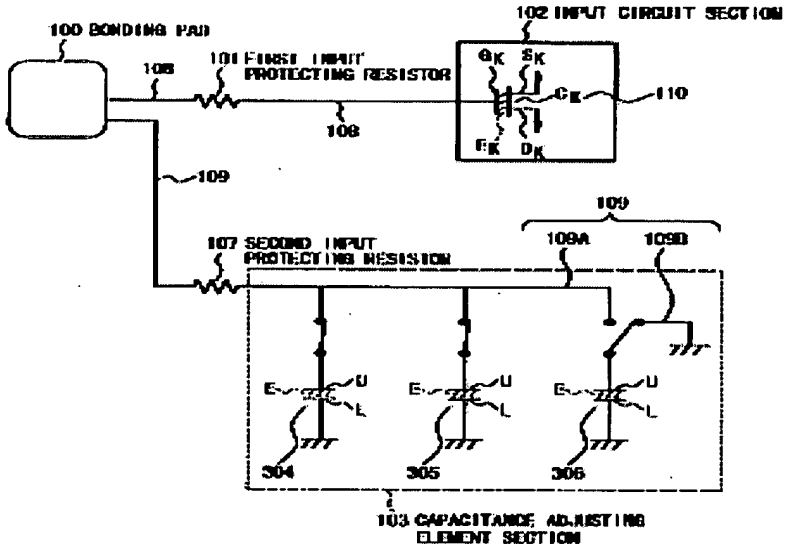
In re claim 9, **Matsui** discloses that the semiconductor integrated circuit device according to Claim 8, wherein the well potential control section comprises: a plurality of resistors **101, 107** which are connected in series to each other between two potential electrodes; and a plurality of switches **104, 105, 106** each of which is connected in parallel to each of the plurality of resistors (FIG. 3),

the well potential control section controls the well region potential by controlling each one of the plurality of switches **104, 105, 106** (col. 7, line 66 to col. 8, line 29).

In re claim 10, **Matsui** discloses that the semiconductor integrated circuit device according to Claim 9, further comprising: a plurality of the terminals **100**; and a plurality of the first capacitance adjusting sections **103** each of which is connected to each of a plurality of the wirings **108, 109** between each of the plurality of terminals **100** and each of a plurality of the protection resistors **101, 107**, wherein the well potential control section controls each of a plurality of said well region potentials (col. 7, line 39 to col. 8, line 65 and FIG. 3).

In re claim 11, **Matsui** discloses that the semiconductor integrated circuit device according to Claim 1, further comprising: a second capacitance adjusting section which is connected to a wiring between the first capacitance adjusting section and the internal circuit, wherein the second capacitance, adjusting section adjusts the terminal capacitance based on capacitance of the second capacitance adjusting section; and a switching control section which controls the capacitance of the second capacitance adjusting section (FIG. 5).

Fig. 5



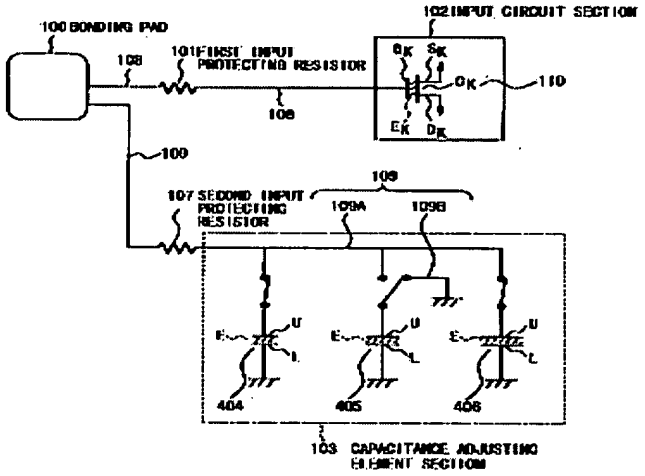
In re claim 12, **Matsui** discloses that the semiconductor integrated circuit device according to Claim 11, wherein the switching control section comprises: a plurality of switches **104, 105, 106** each of which outputs signal potentials corresponding to turn on and off of the each of plurality of switches, and a plurality of signal holding sections each of which holds corresponding each of a plurality of the signal potentials wherein the switching control section controls the capacitance of the second capacitance adjusting section based on the plurality of signal potentials (FIG. 4).

In re claim 13, **Matsui** discloses that the semiconductor integrated circuit device according to Claim 12, wherein the second capacitance adjusting section comprises: a plurality of third adjusting capacitors each of which capacitance is variable based on corresponding each of the plurality of signal potentials, wherein the second capacitance

adjusting section adjusts the plurality of third adjusting capacitors based on the plurality of signal potentials (FIG. 4).

In re claim 14, **Matsui** discloses that the semiconductor integrated circuit device according to Claim 13, further comprising: a plurality of said terminals; and a plurality of the second capacitance adjusting sections each of which is connected to each of a plurality of the wirings between each of the plurality of the first capacitance adjusting sections and each of a plurality of the internal circuits, wherein the switching control section controls each of a plurality of said capacitances of the plurality of second capacitance adjusting sections (col. 4, line 54 to col. 11, line 10 and FIG. 6).

Fig. 6



In re claim 15, **Matsui** discloses that the semiconductor integrated circuit device according to Claim 3, further comprising: a second capacitance adjusting section which is connected to a wiring between said first capacitance adjusting section and said internal circuit, wherein the second capacitance adjusting section adjusts the terminal capacitance based on capacitance of the second capacitance adjusting section; and a switching control

section which controls said capacitance of said second capacitance adjusting section (col. 10, line 54 to col. 11, line 10 and FIG. 6).

In re claim 16, **Matsui** discloses that the semiconductor integrated circuit device according to Claim 15, wherein the switching control section comprises: a plurality of switches each of which outputs signal potentials corresponding to turn on and off of each of plurality of switches, and a plurality of signal holding sections each of which holds corresponding each of a plurality of said signal potentials, wherein the switching control section controls the capacitance of the second capacitance adjusting section based on the plurality of signal potentials (FIG. 6).

In re claim 17, **Matsui** discloses that the semiconductor integrated circuit device according to Claim 16, wherein the second capacitance adjusting section comprises: a plurality of third adjusting capacitors each of which capacitance is variable based on corresponding the each of the plurality of signal potentials, wherein the second capacitance adjusting section adjusts the plurality of third adjusting capacitors based on the signal potential (col. 10, line 54 to col. 11, line 10 and FIG. 6).

In re claim 18, **Matsui** discloses that the semiconductor integrated circuit device according to Claim 17, further comprising: a plurality of said terminals; and a plurality of the second capacitance adjusting sections each of which is connected to each of a plurality of the wirings between each of the plurality of the first capacitance adjusting sections and each of a plurality of the internal circuits, wherein the switching control section controls each of a plurality of the capacitances of the plurality of second capacitance adjusting sections (col. 10, line 54 to col. 11, line 10 and FIG. 6).

Allowable Subject Matter

Claims 4-6 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Khiem D. Nguyen whose telephone number is (571) 272-1865. The examiner can normally be reached on Monday-Friday (8:30 AM - 5:30 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on (571) 272-1855. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

K.N.
June 24th, 2005

W. DAVID COLEMAN
PRIMARY EXAMINER